Capacitance of TSVs in 3-D Stacked Chips a Problem? Not for Neuromorphic Systems!

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ABSTRACT

In order to cope with increasingly stringent power and variability constraints, architects need to investigate alternative paradigms. Neuromorphic architectures are increasingly considered (especially spike-based neurons) because of their inherent robustness and their energy efficiency. Yet, they have two limitations: the massive parallelism among neurons is hampered by 2D planar circuits, and the most cost-effective hardware neurons are analog implementations that require large capacitors, We show that 3D stacking with Through-Silicon-Vias applied to neuromorphic architectures can solve both issues: not only by providing massive parallelism between layers, but also by turning the parasitic capacitances of TSVs into useful capacitive storage.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types & Design Styles - Advanced technologies

General Terms

Design

Keywords

3D architectures, Neuromorphic systems, analog circuits

1. INTRODUCTION

Due to increasingly stringent energy constraints (i.e., Dark Silicon [4]), heterogeneous multi-cores composed of a mix of cores and energy-efficient accelerators are becoming mainstream. However, on top of energy constraints, defects are becoming prominent constraints as well, so that the research focus is progressively shifting to designing energy-efficient *and* defect-tolerant accelerators. Interestingly, these technology constraints come at a time where high-performance applications experience a dramatic shift of their own, from scientific computing applications to *Recognition, Mining, Synthesis* applications, as coined by Intel [2]. And few approaches are better positioned than *neuromorphic architectures* to tackle Recognition and Mining applications while providing inherent defect-tolerant and energy-efficient properties, as recently illustrated by the IBM Cognitive Chip [1].

Thanks to very efficient coding of information, spiking neurons are usually considered to be the neuron model with the greatest potential for applications. Analog neurons have a significantly smaller area footprint than digital neurons because they can leverage physics laws for implementing several elementary functions (see Figure 1): temporal integration is realized through capacitive integration, weight summation through Kirchhoff's law, and leakage is an intrinsic behavior of microelectronic devices.

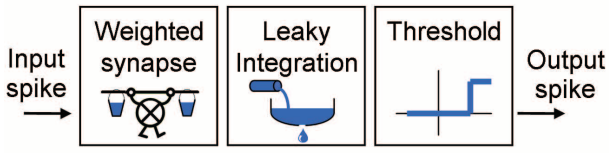

Figure 1: Block diagram of a leaky-integrate-and-fire neuron spiking neuron: weighted summation, temporal integration with leakage, and threshold.

However, analog spiking neuron implementations suffer from two limitations. First, they require large capacitances to store the internal membrane voltage of the neuron. Typical capacitances values are in the order of $0.5-1\ pF$, which corresponds to $50-200\ \mu m^2$ capacitors in $32-65\ nm$ technologies, and up to 50% of the total neuron area. Second, neuromorphic architectures at large are fundamentally 3D structures with massive parallelism, but the 2D planar circuits on which they are implemented considerably limit the bandwidth between layers (or significantly increase the area and energy cost required to achieve sufficient bandwidth).

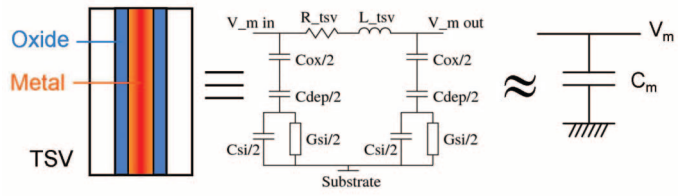

Figure 2: TSV structure and electrical model.

Both issues can be addressed with 3D stacking. It provides massive parallelism between layers by stacking and directly

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connecting them via a large number of Through-Silicon Vias (TSVs). Normally, these TSVs are a significant limitation of 3D stacking: they consume on-chip area and suffer from parasitic capacitances [3]. However, we can actually take advantage of these capacitances to implement the capacitors of spiking neurons, turning a weakness into a useful feature.

2. TSV MODEL

Through Silicon Vias are used to create vertical interconnections in 3-D stacked chips. As shown in Figure 2, they are composed of a metal wire isolated from the substrate. They are not perfect wires however, and act as MOS capacitors. We use an RLC π-shaped electrical model of TSVs as described in [3] (see Figure 2, middle). The TSV model features a resistance R_{tsv}, and an inductance L_{tsv}. It is isolated from the substrate by three capacitors C_{ox}, C_{dep} and C_{si}, while parasitic silicon substrate losses are represented by a conductance G_{si}. All of these values are process dependent and can change with TSV density, height, diameter, operating frequency and oxide thickness.

3. NEURON DESIGN AND SIMULATION

We designed an analog leaky integrate-and-fire neuron using the TSV model presented in Section 2 (TSV-neuron), and compared it through Spice simulations against a neuron using a standard capacitor. Figure 3 shows the behavior of the neuron internal potential V_m for standard (top) and TSV (bottom) neurons (for different densities). When V_m reaches a threshold voltage V_{th}, V_m is reset to a resting potential. With a medium density TSV ($400/mm^2$), it can be seen that the TSV-neuron exhibits the exact same behavior as the standard neuron. TSVs with other densities exhibit similar behavior, albeit with different time constants.

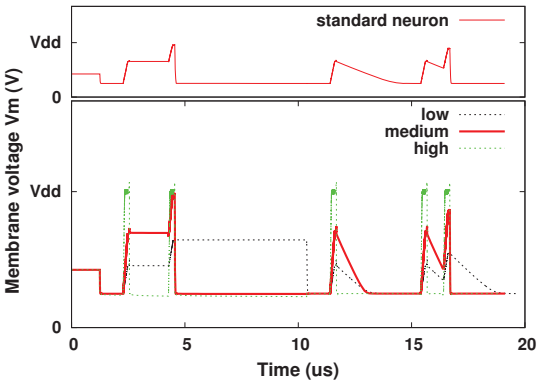

Figure 3: Membrane potential of standard- and TSV-based (several TSV densities) neurons.

4. ARCHITECTURAL OPPORTUNITIES

In Figure 4, we give examples of neuron connectivity and silicon area. Each neuron is composed of three blocks: weight injection, capacitance, and threshold detection (see Figure 1), respectively of areas $A/4$, $A/2$ and $A/4$, considering a standard neuron with area A. These blocks are respectively represented in orange, red and blue in Figure 4. TSVs can either be classically used as wires to transmit information (b), or be used as capacitive elements (c,d). Topology (c) splits neurons into two halves on each side of the TSV; topology (d) embeds both weight injection and threshold detection on both layers around the TSVs, allowing the neuron to operate on each layer, thus dramatically increasing connectivity. In Table 1, we show the area and connectivity gains that can be expected. Two areas are considered: one is the total silicon footprint of a neuron, the other is its required mask area. For topologies (c) and (d), the same mask set can be re-used for each layer in the 3D stack, thus reducing the neuron footprint on mask layers costs.

Table 1: Expected gains

Topology	(a)	(b)	(c)	(d)
Silicon footprint	A	A	A/2	A
Mask set footprint	A	A	A/4	A/2
Connectivity	4 IOs	6 IOs	4 Is & 4 Os	8 IOs

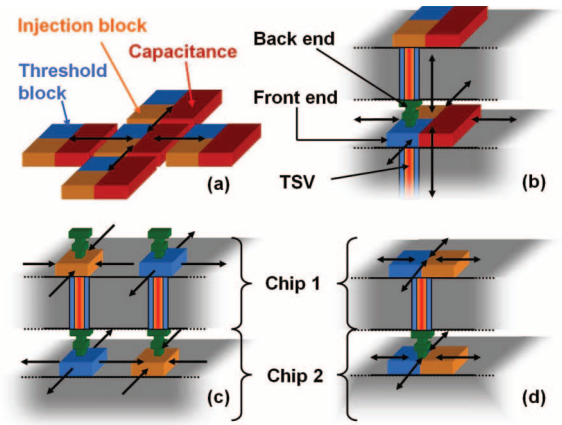

Figure 4: Illustrations of (a) a standard 2D neuromorphic architecture (b) a 3D-IC with standard 2D neurons, and (c) (d) a 3D-IC with TSV-based neurons.

5. DISCUSSION

We showed that it is possible to take advantage of TSVs for implementing the capacitive functionality of spiking neurons in neuromorphic architectures, dramatically increasing density and connectivity. TSVs with different characteristics (length, width, and pitch) could serve various needs: compact TSVs to quickly transmit information from one die to another; large TSVs to act as capacitors while still transmitting information vertically. While TSV-based capacitors are subject to substrate noise and might thus be influenced by neighboring TSVs [5], this phenomenon could again be leveraged to transmit information among neighboring neurons, in the spirit of local field potentials in biological systems.

6. REFERENCES

[1] G. Brumfiel. Inside ibm's cognitive chip. *Nature News*, Aug 2011.

[2] P. Dubey. Recognition, mining and synthesis moves computers to the era of tera. *Technology at Intel Magazine*, 09, Feb 2005.

[3] C. Fuchs, J. Charbonnier, and S. Cheramy. Process and RF modelling of TSV last approach for 3D RF interposer. *IITC/MAM 2011*, pages 9–11, 2011.

[4] M. Muller. Dark Silicon and the Internet. In *EE Times "Designing with ARM" virtual conference*, 2010.

[5] R. Weerasekera et al. Compact modelling of through-silicon vias (TSVs) in three-dimensional (3-D) integrated circuits. In *Proc. IEEE Int. Conf. on 3D System Integration (3D IC)*, pages 1–8, 2009.