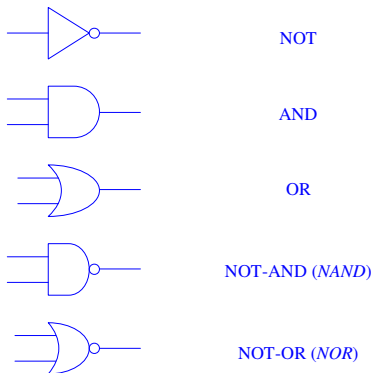


Logic Circuits

Elementary Logic Rules and Theorems

- Boolean algebra
- Axioms
 - commutativity: $a \text{ ET } b = b \text{ ET } a$, $a \text{ OU } b = b \text{ OU } a$
 - associativity: $a \text{ ET } (b \text{ ET } c) = (a \text{ ET } b) \text{ ET } c$, $a \text{ OU } (b \text{ OU } c) = (a \text{ OU } b) \text{ OU } c$
 - distributivity: $a \text{ ET } (b \text{ OU } c) = a \text{ ET } b \text{ OU } a \text{ ET } c$, $a \text{ OU } (b \text{ ET } c) = (a \text{ OU } b) \text{ ET } (a \text{ OU } c)$
 - identity element: $\text{VRAI ET } a = a \text{ ET VRAI} = a$, $\text{FAUX OU } a = a \text{ OU FAUX} = a$
 - complement: $a \text{ ET } a' = \text{FAUX}$, $a \text{ OU } a' = \text{VRAI}$
- Theorems
 - $a \text{ ET FAUX} = \text{FAUX}$, $a \text{ OU VRAI} = \text{VRAI}$
 - $a \text{ ET } (a \text{ OU } b) = a$, $a \text{ OU } (a \text{ ET } b) = a$
 - $a \text{ ET } a = a$, $a \text{ OU } a = a$
 - $(a')' = a$
 - De Morgan: $(a \text{ ET } b)' = a' \text{ OU } b'$, $(a \text{ OU } b)' = a' \text{ ET } b'$
- Shannon's results
- Logic information coding: TRUE/FALSE \rightarrow 1/0
- Notation:
 - AND $\rightarrow \cdot$
 - OR $\rightarrow \dagger$

Elementary Gates Schematic



The Transistor

$G = V_{DD}/1 \Rightarrow V_2 = V_1$

Gate G —

Type *n*

$G = V_{SS}/0 \Rightarrow V_2 = V_1$

Gate G —

Type *p*

- Transistor \approx Switch
- Transistors *n* et *p*.

Simple Logic Functions Using Transistors

$A \rightarrow Z$

$A, B \rightarrow Z$

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

NAND

Simple Logic Functions Using Transistors

$A, B \rightarrow Z$

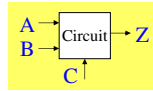
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

AND

Logic Circuit Design

C	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

$C=0 \Leftrightarrow C'$
 $A=1 \Leftrightarrow A$
 $C=0 \text{ AND } A=1 \text{ AND } B=0 \Leftrightarrow C'.A.B'$
 $Z=1 \Leftrightarrow C'.A.B' + C'.A.B + C.A'.B + C.A.B$



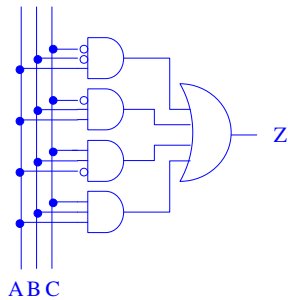
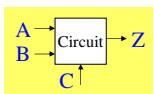
Truth Table

$$Z = C'.A.B' + C'.A.B + C.A'.B + C.A.B$$

Example:

- Input: two binary signals A and B, and control signal C;
Output: Z.
- If C=0, Z=A; If C=1, Z=B

Logic Circuit Design



$$Z = C'.A.B' + C'.A.B + C.A'.B + C.A.B$$

Simplifying Boolean Expressions

- Circuit cost:
 - Number of gates
 - Number of inputs (*fan-in*) and outputs (*fan-out*)
- A few simplification rules:
 - $XY + XY' = X$
 - $X + X'Y = X + Y$
 - $XY + X'Z + YZ = XY + X'Z$ (consensus)

Previous example:

$$\begin{aligned}
 S &= AB'C' + ABC' + A'BC + ABC \\
 &= AC'(B+B') + BC(A+A') \\
 &= AC' + BC
 \end{aligned}$$

Karnaugh Maps

- An intuitive tool for circuits with few inputs
- Different spatial arrangement of 0s/1s than in truth table
- Group two neighbor 1s \Leftrightarrow remove a variable and a term
- Function = covering all 1s = OR of all 1s

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

Truth table

B\A	0	1
0	1	1
1	1	0

Karnaugh map

$$\begin{aligned}
 &A'B' + AB' + A'B \\
 &= A'B' + AB' \\
 &+ A'B' + A'B \\
 &= B' + A'
 \end{aligned}$$

Karnaugh Maps with 3 and 4 variables

- Expression of two neighbor cells identical except for one variable
- Covering using heuristic.
- Quine-McCluskey more scalable

BC\A	0	1
00	1	1
01	0	1
11	1	1
10	1	1

$Z = A + B + C'$

CD\AB	00	01	11	10
00	1	0	0	1
01	0	0	0	1
11	1	1	0	0
10	1	1	0	1

$Z = A'C + B'D' + AB'C'$

Un-Assigned Values

- Output value not defined (case does not exist)
- Notation = **X** or **d** (don't care).
- Can be covered if allows further simplification

CD\AB	00	01	11	10
00	1	0	X	1
01	X	0	X	1
11	1	1	0	0
10	1	1	0	1

$Z = A'C + B'D' + AC'$

Example

C	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Truth table

AB\C	0	1
00	0	0
01	0	1
11	1	1
10	1	0

$$Z = AC' + BC$$
