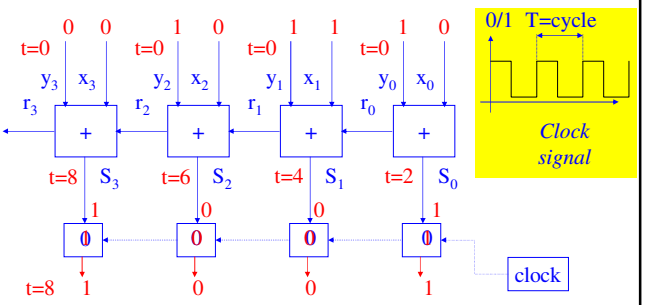
Time and Storage

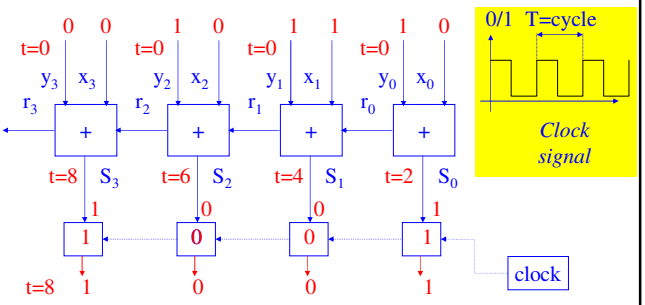
Time



- Synchronization:
  - Wait for the output of all adders to be valid before propagating result
  - Estimate computation time to find appropriate delay
- Insert « barriers » to synchronize outputs

→ Control of « barriers »: **clock**, periodic signal

Why do you need Time ?



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  - Wait for the output of all adders to be valid before propagating result
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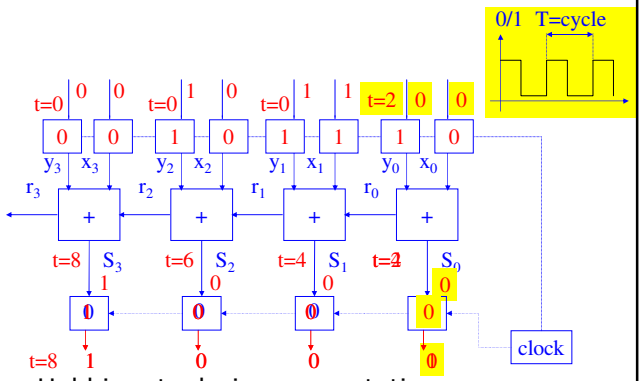
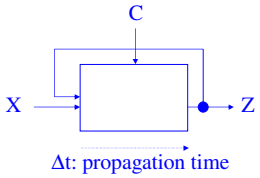
Why do you need Memory ?



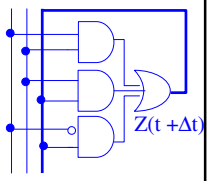
- Hold inputs during computation → memory

How To Implement A Memory Circuit ?

C	X	Z(t)	Z(t+Δt)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

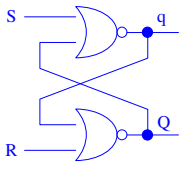


$$Z(t+\Delta t) = C'.Z(t) + X.Z(t) + C.X$$



- Barrier: input X, output Z, control using clock C:
  - C=0: memory → Z(t+Δt) = Z(t)
  - C=1: propagate information → Z(t+Δt) = X
- Loop: send output to input → **memory**

Latches

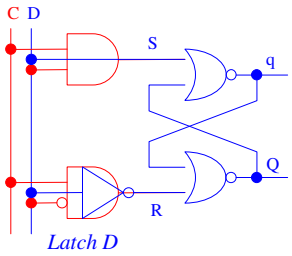


Latch SR

S	R	Q	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	*d*
1	1	1	*d*

- Memorization circuits used as "building blocks"
- Different types of latches (number of control signals and behavior)
- SR= *Set*/*Reset*: memorize or set 1/0.

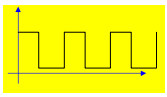
Latches



Latch D

C	D	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

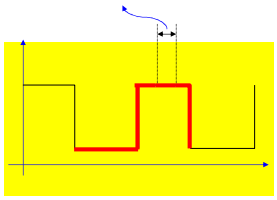
- Latch D: *Delay*, memorization circuit only
- Adding clock:
  - C=0 → memorization
  - C=1 → open

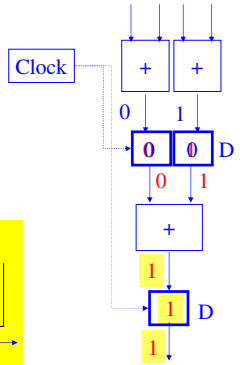


Flips-Flops

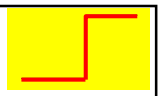
- Operators/Computations usually in sequence
- A latch can store a result but not truly separate two operators

1-bit adder delay

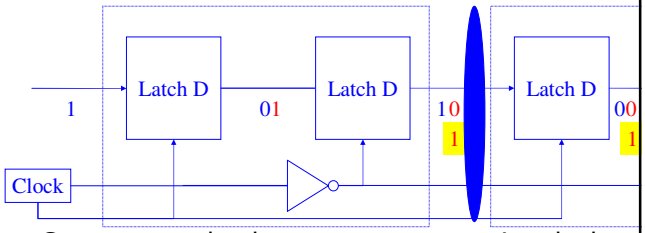




Flips-Flops



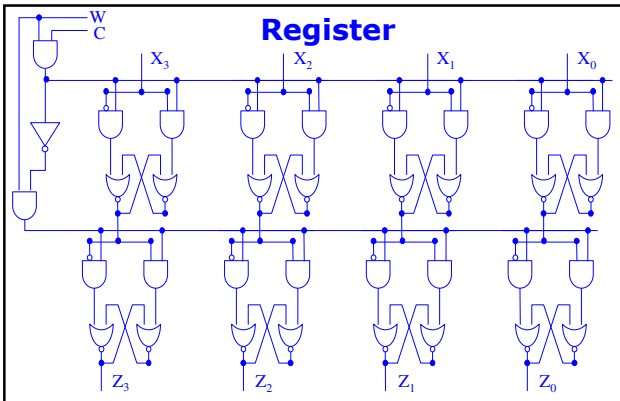
Flip-Flop D



- Connect two latches, open on opposite clock phases:

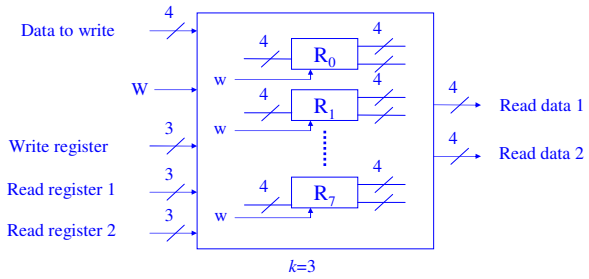
  ⇒ The signal can only go through one of the two latches (≈ air lock).

Register



- *n* flip-flops D in parallel
- Storing one word
- Read/Write; signal *W*=1 → Write

Register Bank



- Small 2^k – word memory
- Usually, at least 1 write port, 2 read ports
- Access through register number ~ address (*k* bits).